

**ASIA PACIFIC UNIVERSITY OF**

**TECHNOLOGY & INNOVATION**

EE008-3-2-DE DIGITAL ELECTRONICS

GROUP ASSIGNMENT REPORT

TITLE: Digital Timer Group Circuit

**GROUP 7**

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# **Introduction**

A digital clock timer is an electronic device or application that shows the time digitally and may measure and display elapsed time or countdown to a certain period or length. It usually has a digital display that shows the hours, minutes, and sometimes seconds.

Digital clock timers are extensively used in a variety of situations, including restaurants, schools, sporting events, and labs, to accurately measure time and offer visual clues for time management. They often include buttons or controls that let users to specify the desired time or length and start or stop the countdown.

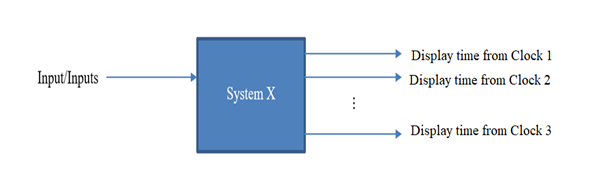
These timers can be freestanding devices with their own power supply or integrated into other devices such as microwaves, ovens, or cell phones. They supply ease and accuracy.

Our task was to construct a digital timer circuit which displays time in four different formats (30 Minutes, 25 Minutes, 20 Minutes, and 15 Minutes) as well as a 2-bit digital control unit that will receive input to display the time from any of the timers. This report will prove how we designed these circuits and the controller and how we integrated them, also we will show the simulation results and discuss the overall outcomes.

# **Objective**

Investigate a digital timer circuit that consists of four different clocks that display different timings (30 Minutes, 25 Minutes, 20 Minutes, and 15 minutes timer). The system can display the time from any one of the timers and that can be controlled by a 2-bit control input given to the designed digital controller.

Exemplify a control unit circuit that can select and display the time from only ONE timer at a time, out of the integrated timer circuit, as illustrated in Figure below.



# **Individual Circuit Design**

# Mehraz Circuit Design

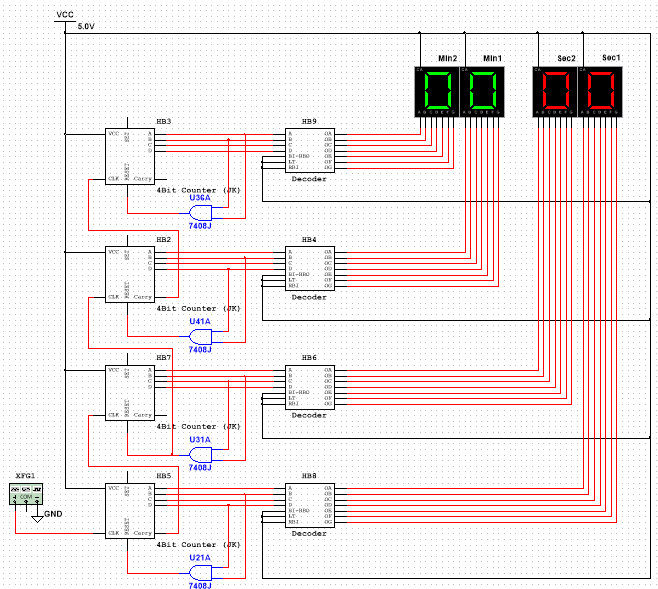
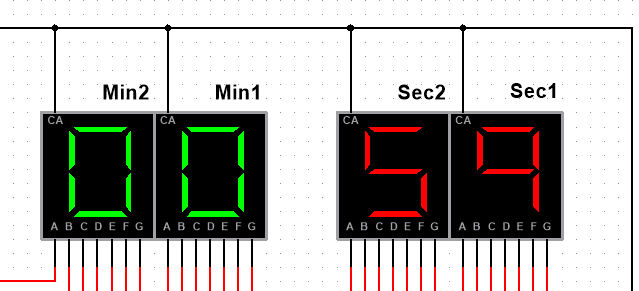
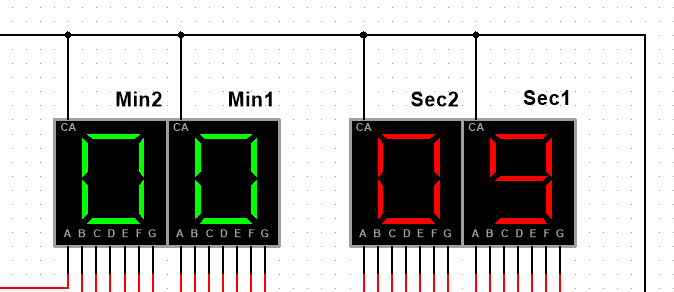


Figure 01: Mehraz’s Individual Circuit

The Circuit designed simulated is illustrated in the Figure above. When the simulation starts, the first and second displays (Sec1&2) combined show a reading up to 59 seconds. On the 60th second, the readings on the displays reset back to zero. After completing the sequence set for seconds, the timer starts counting minutes. After the readings on the second display (Sec1&2) count to 60, it triggers the third display, Min 1. Min 1 reads up to 9 and triggers the next display, Min 2. The minutes displays combined successfully counts to 20 minutes and then resets. The figures below show the readings from the simulation.



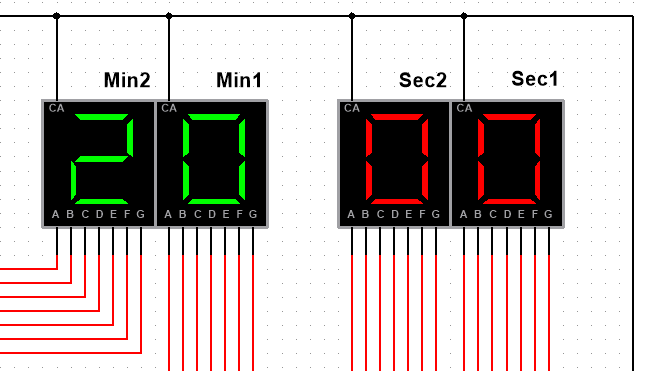
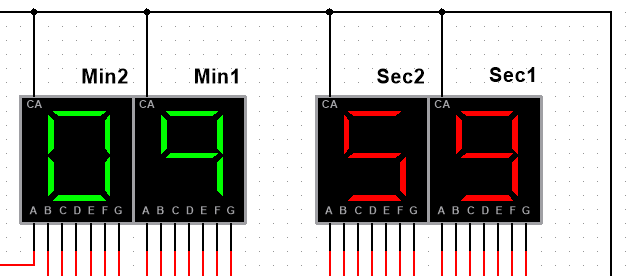


Figure 02: Mehraz’s Individual Circuit Readings

The circuit includes a frequency generator as an input source for the timer, which generates a periodic pulse that starts the counting process. The most crucial part of digital electronics, or timers, are counters, which control the counting sequence and can be used to expand the system's memory. For this project, 4 counters were used to increase the bit size of a 2-bit signal from the frequency generator to a 4-bit output. JK Flip-Flops were used to design the counters. The JK flip-flop must be able to change a single bit of binary data stored in response to the input signals J and K for it to work.

The first and third counters were intended to stop at 9 (1001 in binary), the second counter at 6, and the fourth counter at 2 (0010). This was carried out by including AND gates, which, when both inputs are 1, convert the output from 0 to 1.

The flip flop is programmed to reset when the AND gate output changes from 0 to 1. For instance, when the outputs of B and C are both 1, the AND gate, which is used to stop the counter at 6, will change the output from 0 to 1, resetting the signal. The procedures taken to use the decoder to convert a 4-bit BCD input to a 7-segment output are the most crucial information in this. The final pin (Carry), which changes from 0 to 1, resets the counter. The counters are activated by the change in input at the clock. A display decoder was built to transform the signal; it was modelled after the 7447n IC. The Bi, LT, and RBI conditions must all be set to 1 for the decoder to turn on and supply the desired output. Resistors were also set up to keep control over the current flow.

# Pedro Circuit Design

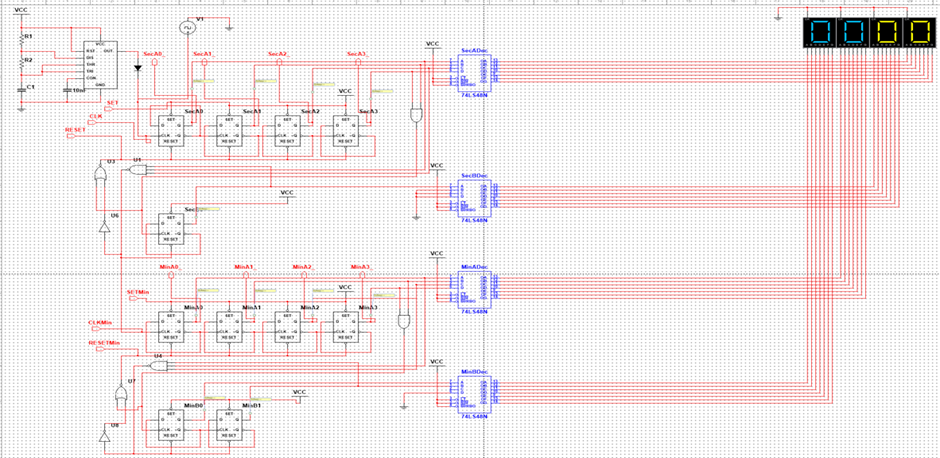


Figure 03: Pedro’s Individual Circuit Readings

Using D Flip-Flops (D-FFs), AND, NAND, NOR, and NOT gates, a minute counter was created. This counter counts to 25 minutes before returning to zero. In addition, for every 15 seconds that pass, it will update once per minute until 25.

As before, we start with D-FFs that all have output Q of 0. The rising edge of the clock activates the first D-FF when a pulse is created. Starting with D = Q = 1, the output Q changes to 1 and D = Q = 0 as a result. With each next rising edge, the output toggles.

The inverse of Q (Q bar) toggles from 0 to 1 when Q's toggle changes from 1 to 0. We can infer that the second D-FF toggles when Q changes from 1 to 0 in the first D-FF since this Q bar signal flows into the clock input of the second D-FF. This creates a 4-bit counter with the following potential states: 0000, 0001, 0010, 0011…, all the way up to 1111, which stands for 15 in binary.

The tens digit, which ranges from 0 to 2, and the ones digit, which ranges from 0 to 5, will be separated into two groups. To create conditions for each digit, we'll use AND, NAND, NOR, and NOT gates. We want the tens digit to count to two (0010 in binary). So, we use a NAND gate to reset the D-FFs when it reaches 3 (0011 in binary). The fourth and fifth bits of the gate are checked to see whether they are both 1, and if they are, the gate sends a reset signal to make 0 the effective potential and a rising-edge signal to the one digit.

Our goal is for the single digit to count to five (0101 in binary). The D-FFs are therefore reset as soon as it reaches 6 (0110 in binary), for instance, when the second and third bits are both 1. When the second and third bits are 1, a NOR gate can recognize this circumstance in this case. A reset signal is supplied to make 0 the effective potential and a rising-edge signal is sent back to the tens digit to restart the count. The NOR gate, which combines the capabilities of OR and NOT gates, does both things. We may feed the output of our seconds counter into the clock input of our minutes counter to make sure that the counter updates every minute for every 15 seconds that have passed. The minutes counter receives a pulse specifically when the second counter hits 15 (1111 in binary).

By applying this reasoning, we can design a counter with digits separated into counts of 2 and 5 that count from 0 to 25 minutes. Each digit counts independently and resets when it reaches its count limit to cause the following digit to increment.

The clock starts counting from zero minutes and zero seconds. It displays two digits for minutes, and seconds.

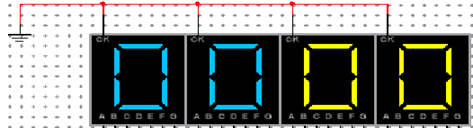


Figure 04: Pedro’s Individual Circuit Readings Clock Starting)

The next second when it reaches 14 minutes and it goes to 15 it will automatically reset from zero as you can appreciate in the excitation table, then, in this case, we can say that it causes a carry to the minute which is going to be updated to 24 minutes as in the case of the next displayed.

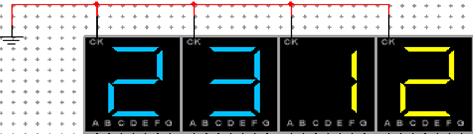


Figure 05: Pedro’s Individual Circuit Readings (Clock 23 minutes and 12 seconds)

Now, for the next displayer once the seconds display reaches 15 it will cause a carry to the minute’s displayer and then a carry to the minutes which is going to go back to reset everything from zero again.

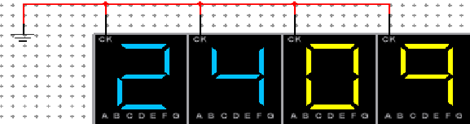


Figure 06: Pedro’s Individual Circuit Readings (Clock at 24 minutes and 9 seconds)

# Helal Circuit Design

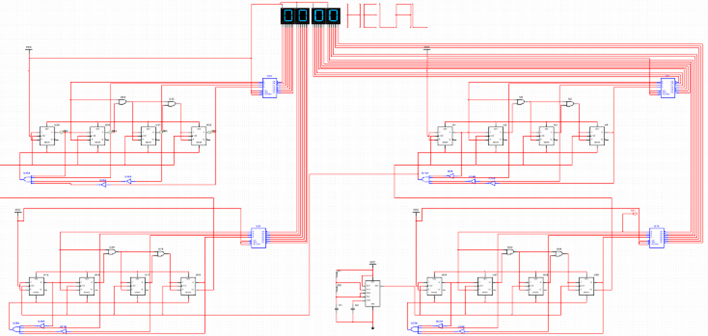


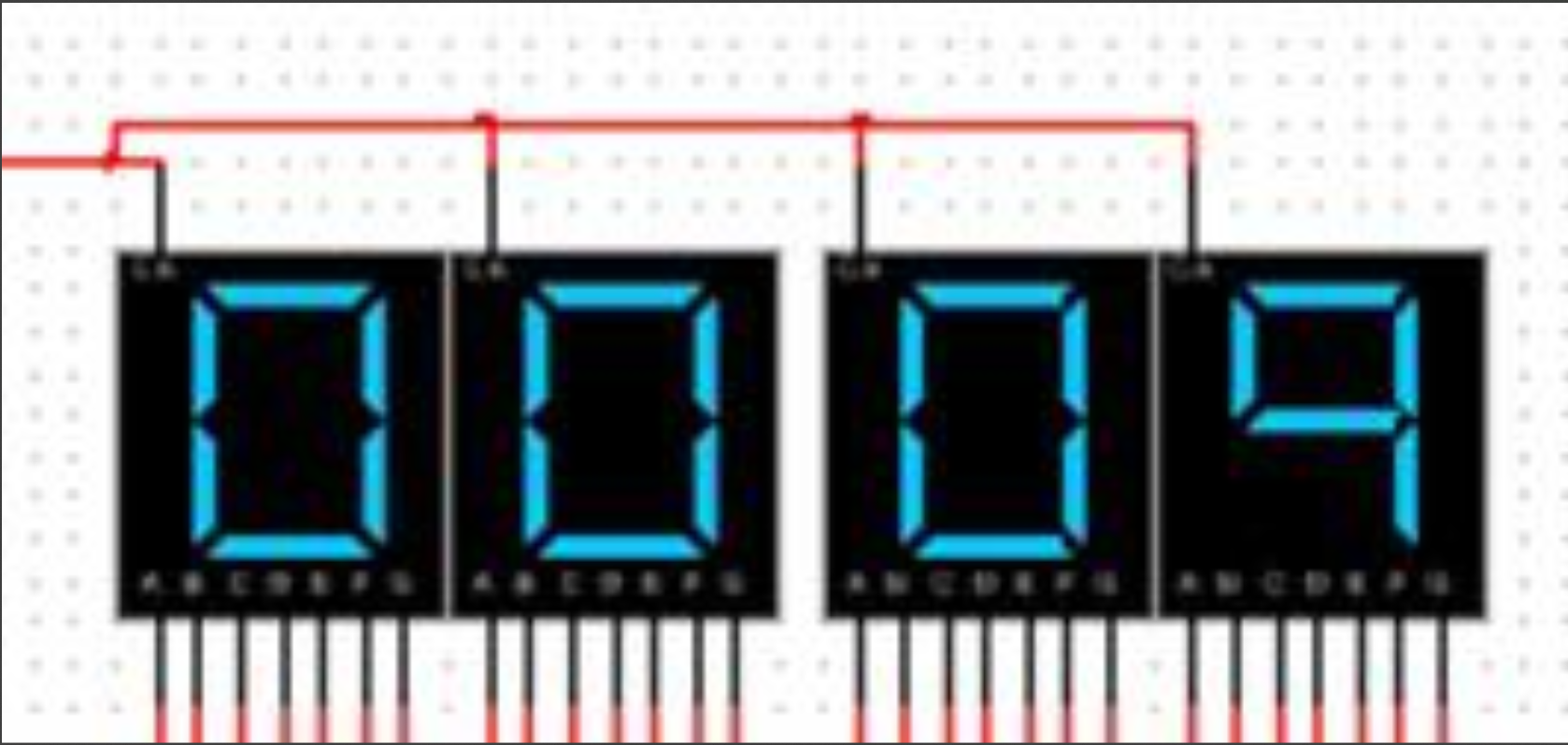
Figure 07: Helal’s Circuit Design

The 30-minute timer circuit's accuracy and dependability in tracking and displaying time intervals are highlighted by the analysis. Throughout rigorous testing, the circuit showed stability and exact timing sequences. An effective and useful timer circuit was created by combining the JK flip-flop, AND gate, NAND gate, 7447N decoder, and seven-segment display.

The digital timer is useful in many contexts, including those that call for precise timekeeping, such as home appliances, and educational materials. In comparison to analogue timers, it is more exact, has a wider range of display formats, and is simpler to integrate.

I learned a lot about circuit design and how digital timers work because of this assignment. My knowledge was improved by having first-hand familiarity with parts like binary decoders and JK flip-flops. I also understood the value of working together to overcome obstacles and enhance the performance of the timer circuit.

My 30-minute timer circuit, in conclusion, is an excellent example of the accuracy and dependability of digital electronics in tracking and displaying time intervals. The project gave students insightful information about circuit design and the practical uses of digital timers. The display interface might be improved, battery consumption could be decreased, and more functions might be investigated. Future versions and improvements will be guided by the input we get through testing and integration.

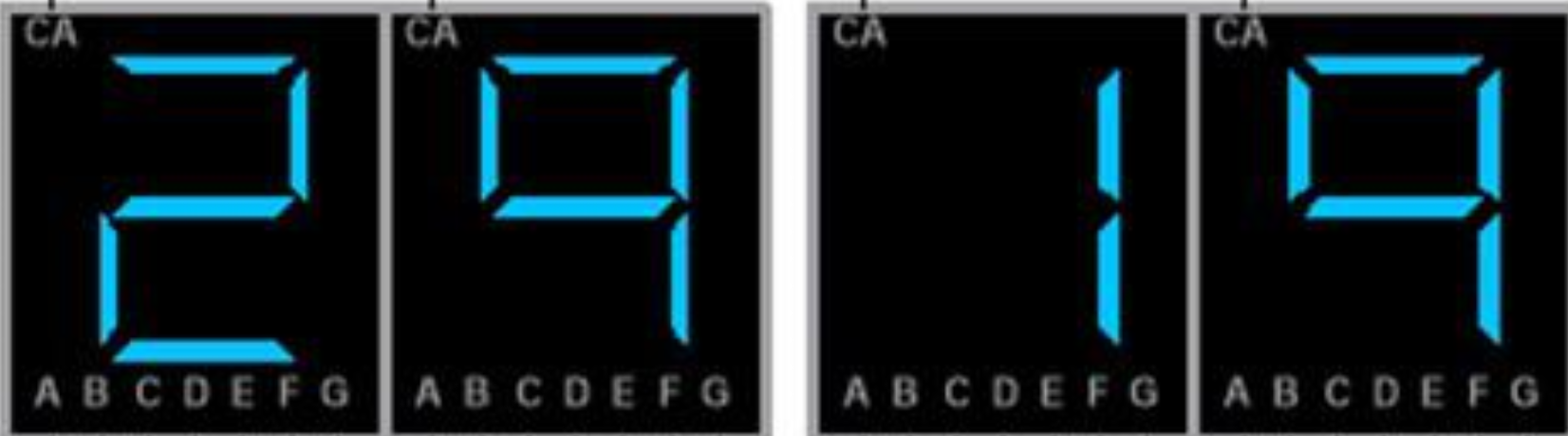


Figure 08: Helal’s Circuit Reading

* Abdullah Circuit Design

A picture containing diagram, text, plan, schematic

Description automatically generated

Figure 09: Abdullah’s Individual Circuit

The figure above shows the circuit design of the counter circuit which was made using JK-flip flops, logic gates, and four 7-segment displays. This counter is a 2-bit asynchronous counter or also known as ripple counter which means the flip-flops are not all clocked by the same clock signal. Instead, each flip-flop is clocked by the output of the earlier flip-flop in the sequence. The output of each flip-flop acts as a clock signal for the next flip-flop in the chain.

When running the circuit, the first counter (seconds counter) will start counting, for this counter it will count from 0 to 40 seconds then it will reset, and when it resets, the second counter (minutes counter) will increase the count by 1 every time the seconds counter reaches 40 secs and resets until it reaches 15 minutes which is the required time for this counter.

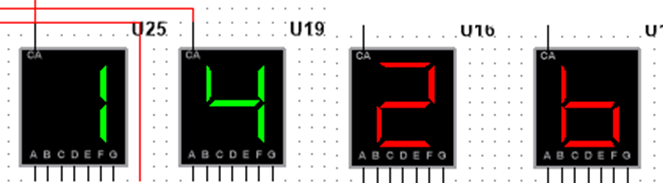


Figure 10: Abdullah’s Individual Circtuit Reading

The seconds are displayed in red, and the minutes are displayed in green. The counter starts from 0 and it keeps incrementing by 1 until it reaches 40 (seconds) before it resets, the reset will trigger the minutes counter which will also keep incrementing by 1 until it reaches 15 (minutes) before resetting back to 0, and as shown in the figure above, the output is displayed clearly and in a readable format without any errors.

The JK-flip flops and logic gates supply a reliable counting mechanism the counter keeps functionality consistently and accurately throughout the entire simulation the counter also transitions smoothly between states without any noticeable glitches or unexpected behavior. Overall, this asynchronous counter simulation produced successful results, with the expected capability of counting from 0 to 15 minutes being achieved.

# **Group Circuit Design**

# Proposed Design

To combine all the circuits of the group members, the proposed system must be flexible. With the use of a control unit, the digital timer should be able to be set to the required timing that is 30, 25, 20 or 15 minutes and 15,20,40 or 60 seconds.

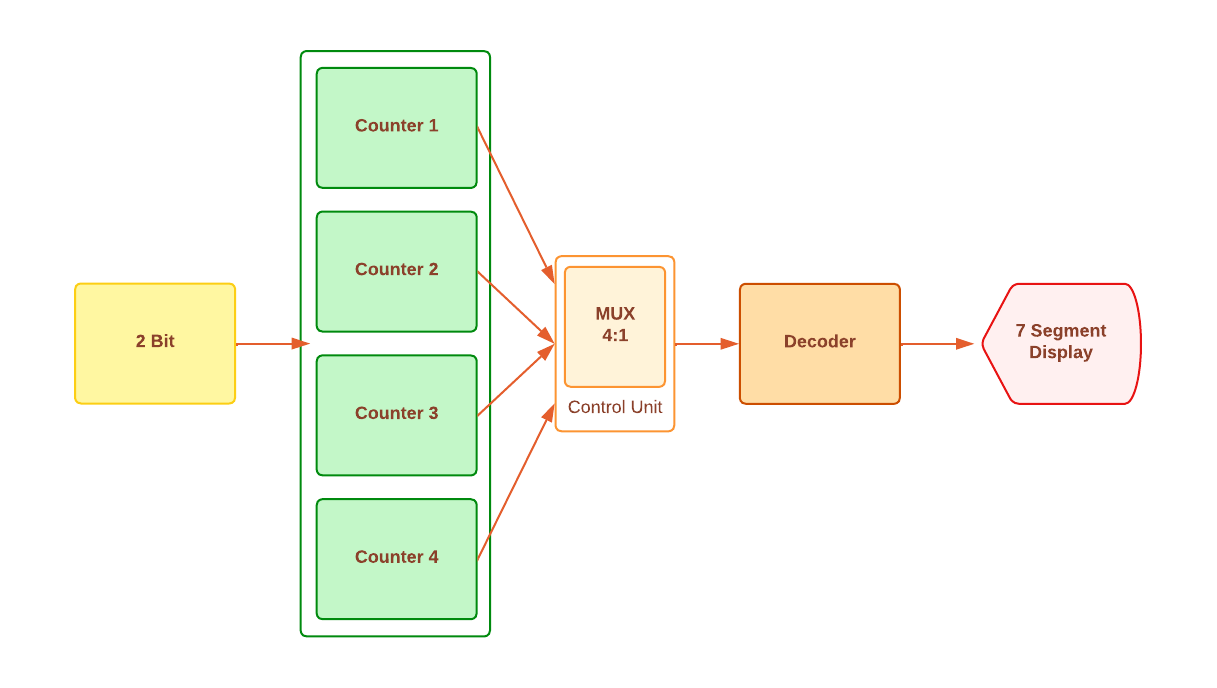


Figure 11: Group Circuit Block Diagram

The block diagram above shows the proposed design that was planned for this project. Individual Circuits were constructed and represented as Counter 1,2,3,4. Each individual circuit is connected to the control unit which will generate an output from the selected counter. The generated 4-bit output is passed though BCD to a 7-segment decoder which then shows the reading on the Display.

# Control Unit

The control unit is constructed using a multiplexer circuit. A multiplexer (MUX) is an electrical part that enables the transmission of multiple input signals via a single output line. Based on the state of the select lines, the multiplexer selects one of the input signals at a time and sends it to the output. As a result, the multiplexer can effectively function as a switch, enabling one signal out of many to flow through at once.

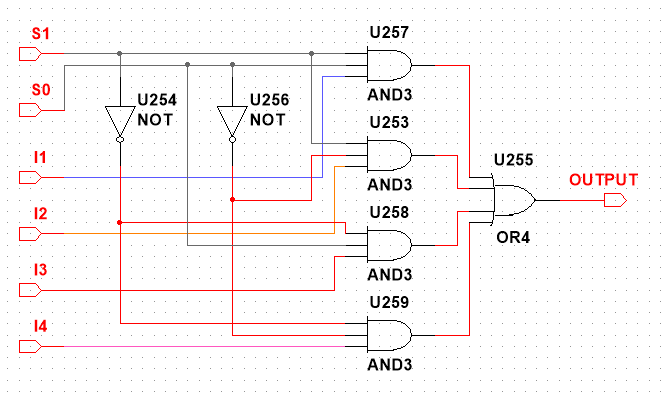


Figure 12: Multiplexer Mux SubCircuit

Above is the sub-circuit of the multiplexer that was constructed for this assignment to combine the circuits. The constructed circuit is a 4:1 Mux that takes 4 inputs and sends only output. The output can be controlled by changing the state of S0 and S1. For example, if S0 is 0, S1 is 0 it will show the first output and if S0 is 0, S1 is 1 the output will be the third output.

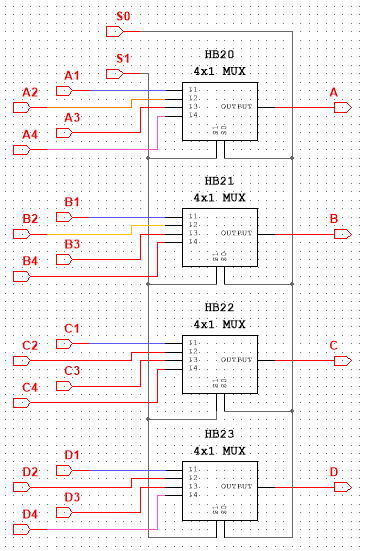
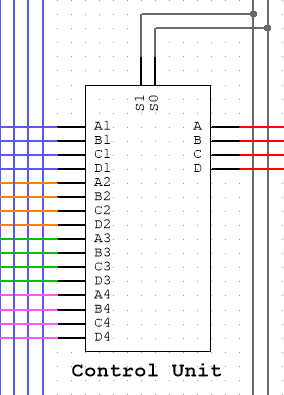


Figure 13: Control Unit SubCircuit

For this group project, 4 timer circuits had to be combined as one. Each individual circuit has 4 counters that generate a 4bit output. To combine the four circuits as one all the 16 outputs are connected to 4 MUX that will give 4 controlled outputs. For Example, each counter from individual circuits gives 4 outputs, A B C D. The output A from the first counter from individual circuit is connected to the first MUX. With different states of S0 and S1, the output from different timer circuits can be called. These steps are followed and the connections to all the multiplexers are made.

The pins A1 B1 C1 D1 from the control unit are connected to Mehraz’s timer circuit, A2 B2 C2 D2 are connected to Pedro’s timer circuit, A3 B3 C3 D3 are connected to Helal’s timer circuit and lastly A4 B4 C4 D4 are connected to Abdullah’s timer circuit.

Table: Truth Table for Control Unit

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| S1 | S0 | ABDULLAH | HELAL | PEDRO | MEHRAZ | OUTPUT |
| 0 | 0 | **A** | 0 | 0 | 0 | **A** |
| 0 | 1 | 0 | **B** | 0 | 0 | **B** |
| 1 | 0 | 0 | 0 | **C** | 0 | **C** |
| 1 | 1 | 0 | 0 | 0 | **D** | **D** |

*Boolean Expression*

# Integrated Design

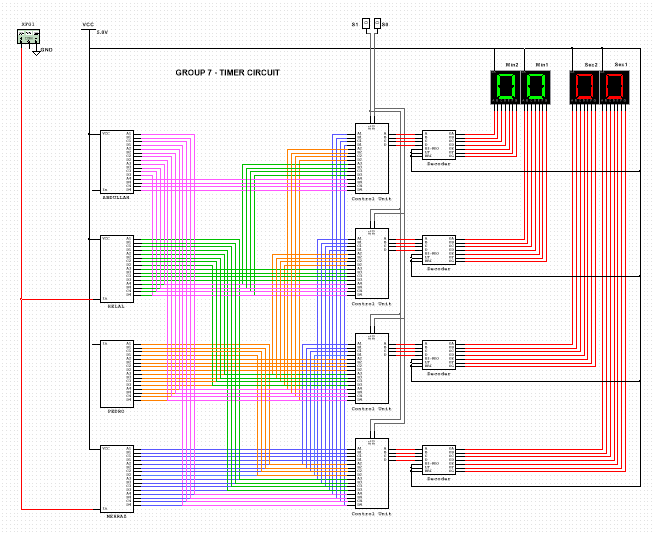


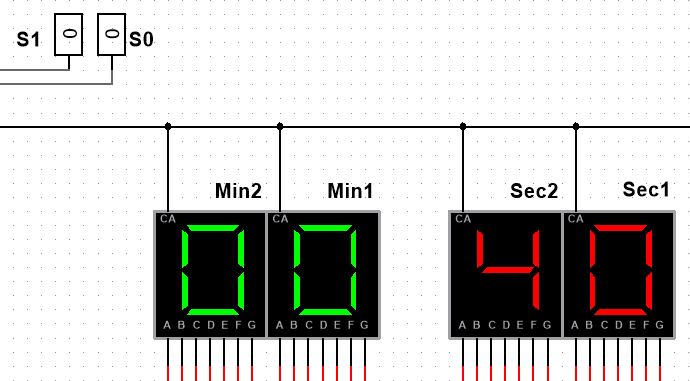
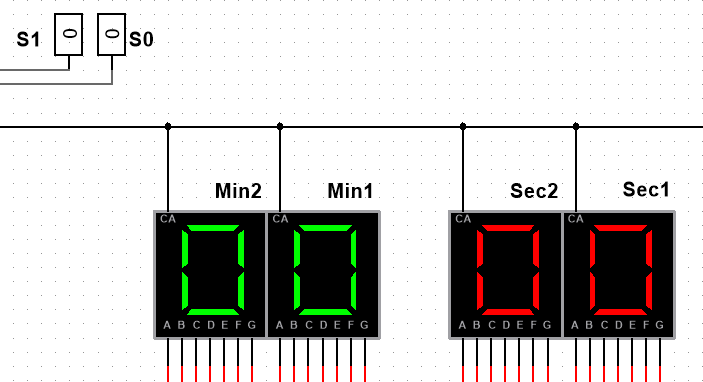
Figure 14: Group Combined Circuit

This is the circuit that was constructed based on the proposed design. The individual circuits are compressed into sub circuits (MEHRAZ, PEDRO, HELAL & ABDULLAH), and the output pins are color coded for ease of understanding of the connections. All the BLUE cables are connected to Mehraz counters, ORANGE cables are connected to Pedro’s counters, GREEN cables to Helal’s counter and lastly all PINK cables are connected to Abdullah’s counter. The control unit is then connected to data switch S0 and S1 that following the truth table above gives the output of the respective counter sub circuits. The output from the control unit is then connected to the decoder which converts the 4bit BCD to 7segment output which is then connected to the 7-segment Display.

# **Simulation Results**

For

***Abdullah (S0 = 0, S1 = 0)***



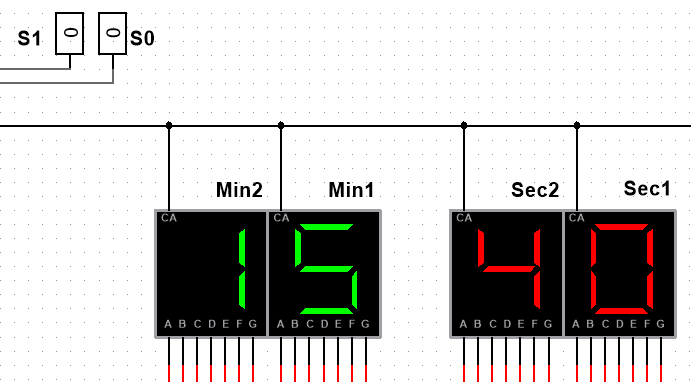
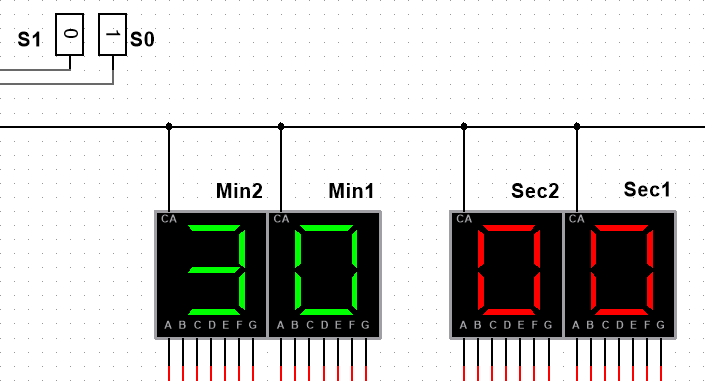
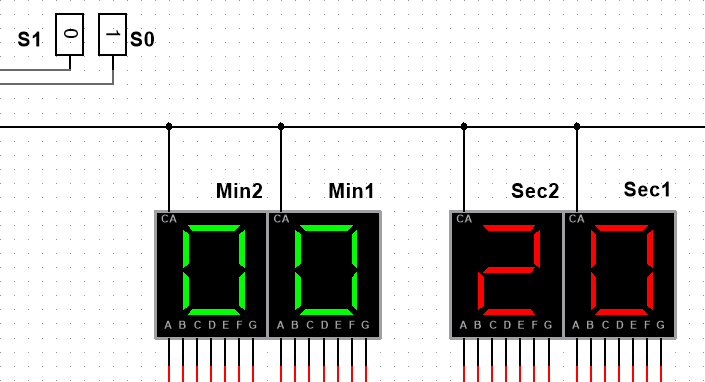


Figure 15: Abdullah’s Circuit Readings from Multiplexer

Abdullah’s Timer Circuit was designed to start counting from 00 minute 00 second till 15 minute 40 Seconds. The seconds timer counts till 40 and resets triggering the minutes timer to count till 15 and reset.

***Helal (S1=0, S0=0)***



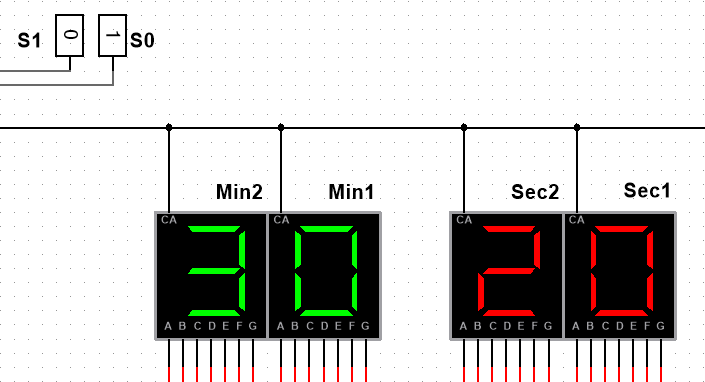
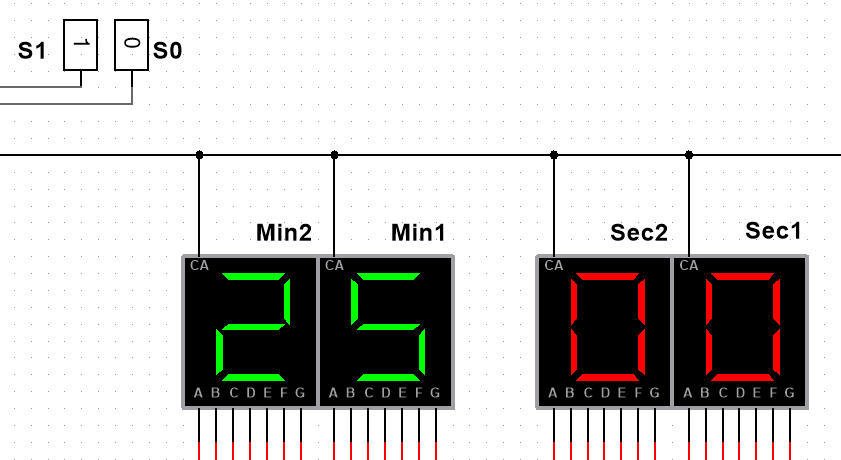
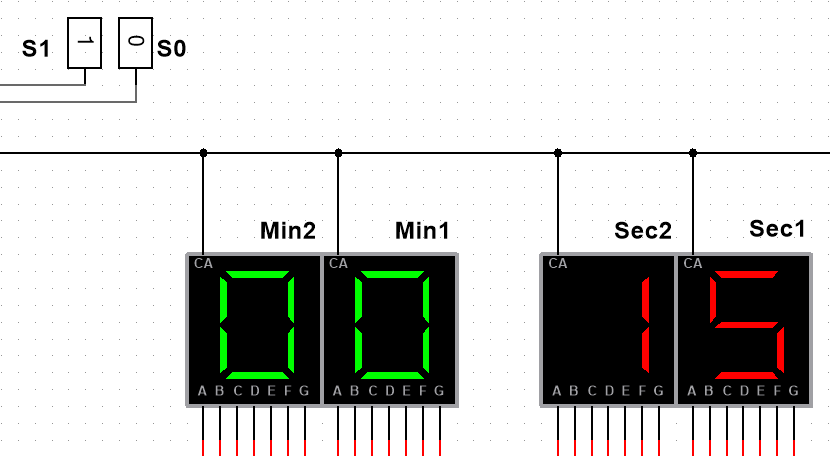


Figure 16: Helal’s Circuit Readings from Multiplexer

Helal’s Timer Circuit was designed to start counting from 00 minute 00 second till 30 minute 20 Seconds. The seconds timer counts till 20 and resets triggering the minutes timer to count till 30 and reset.

***Pedro (S1=0, S0=1)***



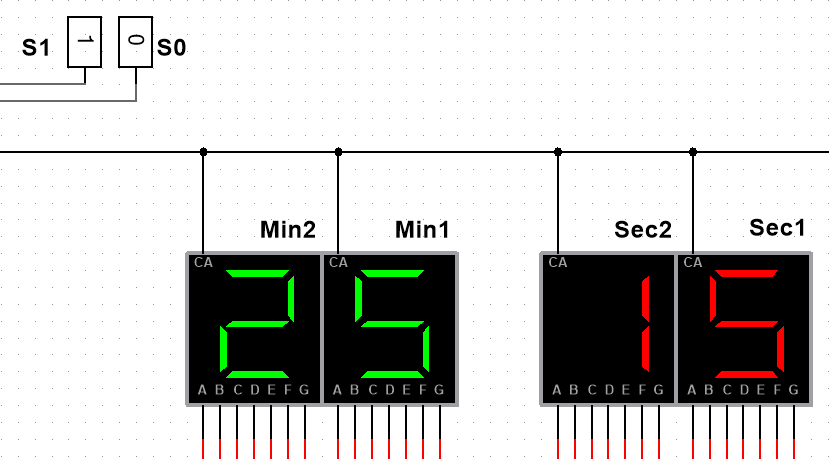
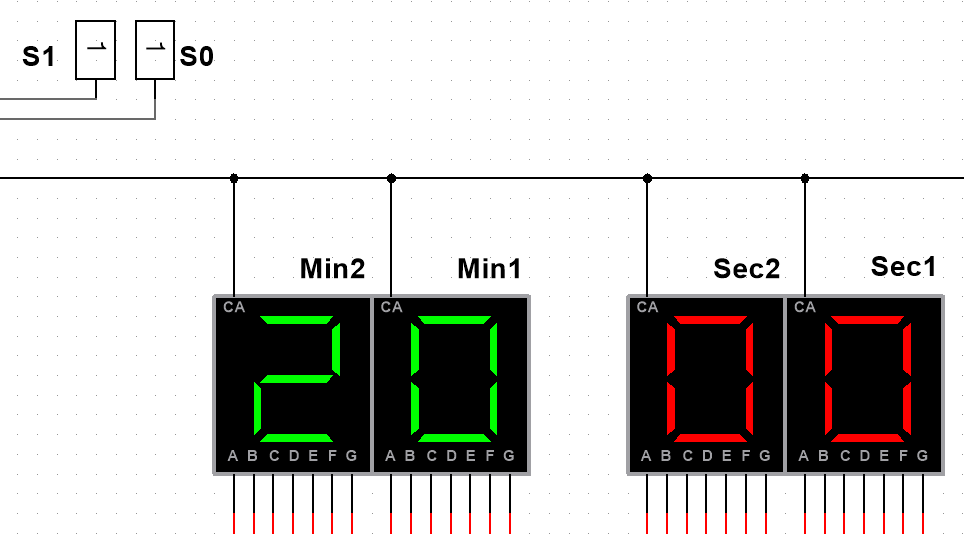
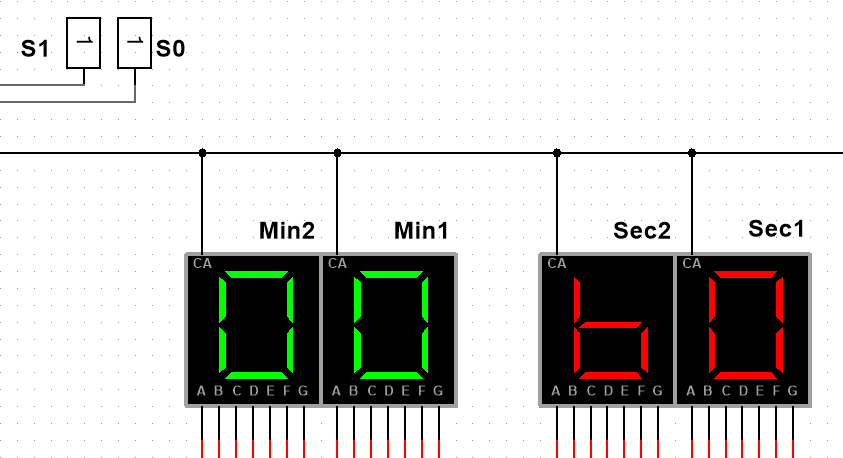


Figure 17: Pedro’s Circuit Readings from Multiplexer

Pedro’s Timer Circuit was designed to start counting from 00 minute 00 second till 25 minute 15 Seconds. The seconds timer counts till 15 and resets triggering the minutes timer to count till 25 and reset.

***Mehraz (S0=1, S1=1)***



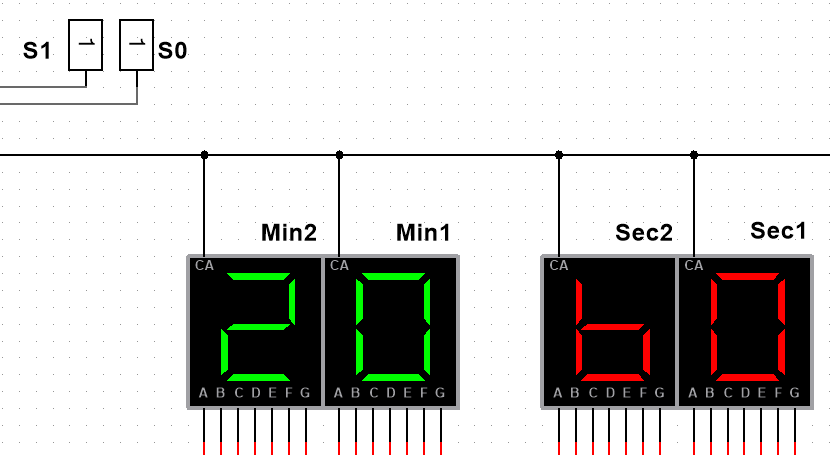


Figure 18: Mehraz’s Circuit Readings from Multiplexer

Mehraz’s Timer Circuit was designed to start counting from 00 minute 00 second till 20 minute 60 Seconds. The seconds timer counts till 60 and resets triggering the minutes timer to count till 20 and reset.

# **Discussion**

Decoder 7447

The 7447 IC has 4 input pins (A, B, C, D) that take a BCD as input, and 7 output pins (a, b, c, d, e, f, g) that output the corresponding 7-segment code. The IC also has three more pins: LT (Lamp Test), BI/RBO (Blanking Input/Ripple Blanking Output), and RBI (Ripple Blanking Input).

LT (Lamp Test): it's set too high (1), which means the display is running normally.

BI/RBO (Blanking Input/Ripple Blanking Output): This pin is used to turn off or blank the display.

RBI (Ripple Blanking Input): This pin is used in conjunction with the RBO pin to blank the display when the input is zero.

These three pins are set to zero and they are connected to VCC which is equal to zero.

It is important to highlight that during the execution of the software we have been facing some significant issues where the system lags when we run it in Multisim. This is likely due to the high complexity of the circuit, which involves many logic gates and sub-circuits. Each of these components requires computational resources to simulate, and when combined, they can cause the simulation to slow down or lag.

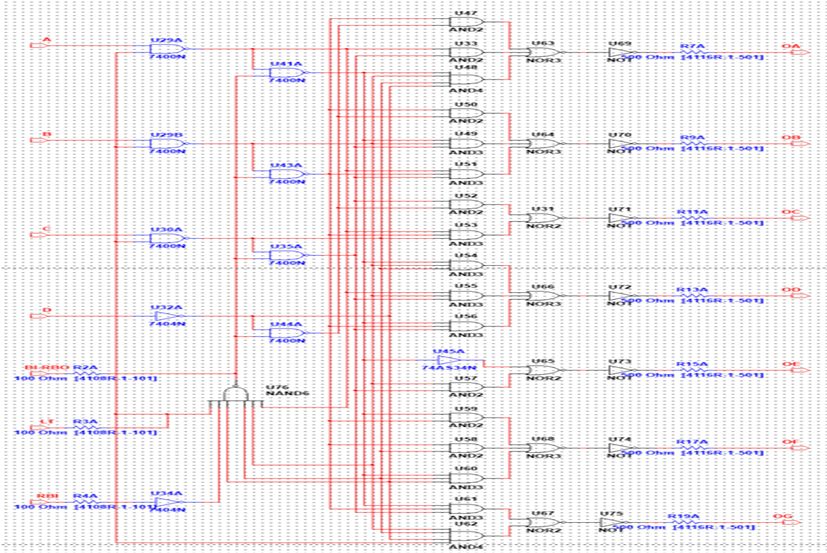


Figure 19: coder’s Circuit Diagram

# **Conclusion**

A control unit was used to set the proper timing intervals of 30, 25, 20, or 15 minutes, along with 15, 20, 40, or 60 seconds, combining all the circuits of the group members into a flexible system. Counters 1, 2, 3, and 4 are individual circuits that were built and connected to the control unit. Each counter produced a 4-bit output that was fed through a BCD to a 7-segment decoder, which displayed the reading on the display.

The multiplexer (MUX) circuit used in the control unit served as a switch, picking one signal at a time based on the status of the select lines. All 16 outputs were connected to 4 MUXs for the integration of the four circuits, creating 4 controlled outputs. The A, B, C, and D outputs of each counter were connected to the corresponding MUX, allowing users to choose between several timing circuits by adjusting the select lines.

In conclusion, the successful integration of the many circuits into a versatile system illustrates the accuracy and flexibility of digital timer circuits. For correct time tracking and display, a control unit, multiplexers, and a BCD to 7-segment decoder are used. Despite the difficulties met during simulation, this research offered insightful knowledge about circuit design and the difficulties of integrating several components. The potential for creating dependable and useful timer solutions is proved by the collaboration, individual contributions, and use of digital electronics.

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